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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,298	12/09/2003	Wagdi W. Abadeer	END920030103US1	3646
30449	7590	07/18/2005	EXAMINER	
SCHMEISER, OLSEN + WATTS			TRA, ANH QUAN	
3 LEAR JET LANE			ART UNIT	
SUITE 201			PAPER NUMBER	
LATHAM, NY 12110			2816	

DATE MAILED: 07/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

**Office Action Summary**

Application No.

10/731,298

Applicant(s)

ABADEER ET AL.

Examiner

Quan Tra

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 June 2005.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3,5-8,10-16,18,19 and 23-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8 and 10-14 is/are allowed.
- 6) ☒ Claim(s) 1-3,5,15,16 and 18 is/are rejected.
- 7) ☒ Claim(s) 6,19 and 23-26 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
 Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/14/05 has been entered.

### ***Claim objection***

Claim 5 is objected because it depends on canceled claim, claim 4.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Phillips et al. (USP 5589784) (previously cited).

As to claims 1 and 15, Phillips et al.'s figure 1 shows a circuit, comprising a tunneling leakage monitor circuit, the tunneling leakage monitor circuit comprising a first PFET (34), a second PFET (36), a first NFET (26) and a second NFET (14); sources of the first and second PFETs connected to a voltage source (Vcc); gates of said first and second PFETs and the drain of the first PFET connected to a drain of the first NFET; a drain of the second PFET connected to a gate of the second NFET; source of the first and second NFETS and a drain of the second NFET

Art Unit: 2816

connected to ground; a current mirror (24) connected to a gate of the first NFET; the current mirror adapted to force a current of a predetermined value from the gate of the second NFET, through a gate dielectric layer of the second NFET through the source and the drain of the second NFET to ground, the current consisting of tunneling leakage current; and an input voltage buffer (39) connected to the gate of the second NFET, the voltage buffer adapted to generate an output based on a voltage level developed across the gate dielectric layer of the second NFET when the current is at the predetermined value.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2, 3 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phillips et al. (USP 5589784) in view of Maneatis (USP 6462527).

As to claims 2 and 16, the modified Hsu et al.'s figure 12 shows all limitations of the claim except for the current mirror includes an adjustable current source and means to adjust a current generated by the current source. However, it is notoriously well known in the art that adjustable current source is more flexible to generate desired current than a fix current source. Maneatis's figure 3 shows an adjustable current source with a large operation range. Therefore, it would have been obvious to one having ordinary skill in the art to use Maneatis' adjustable current source figure 3 for Phillips et al.'s current source for the purpose of having more flexibility to select and generate desired current.

Art Unit: 2816

As to claim 3, the modified Phillips et al. reference further fail to show that the current source is a band gap current source. However, it is notoriously well known in the art that bandgap current source generates current independent of temperature. It would have been obvious to one having ordinary skill in the art to use bandgap current source to provide current to the Maneatis' current mirror circuit for the purpose of improving the performance of the circuit. Maneatis' figure 3 further shows that the means (the switches and the switch selection circuit, not shown, in Maniatis's figure 3) to adjust a current generated by the current source is a digital to analog converter.

6. Claims 5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phillips et al. (USP 5589784) in view of Maneatis (USP 6462527) and Shyr et al. (USP 6472897).

As to claims 5 and 18, the modified Phlipps et al.'s figure 12 shows all limitations of the claim except for fuse circuit controls the DAC. However, Shyr et al.'s figure 1 shows fuse circuit 14 controls the DAC. The benefit of using the fuse circuit is the output control signal irreversible when fuse is blown. Therefore, it would have been obvious to one having ordinary skill in the art to use fuse circuit to control the DAC in the modified Hsu et al.'s reference for the purpose of permanently closing or opening the switches in the DAC.

***Allowable Subject Matter***

7. Claims 8 and 10-14 are allowed.

8. Claims 6, 19 and 23-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Art Unit: 2816

Claims 8 and 10-14 are and claims 6, 19, 24 and 26 would be allowable because the prior art fails to teach or suggest a voltage regulator coupled to the buffer circuit.

Claims 23 and 25 would be allowable because the prior art fails to teach the detail of the buffer circuit as claimed.

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



QUAN TRA  
PRIMARY EXAMINER  
ART UNIT 2816

July 14, 2005